UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,343	06/21/2001	Hosagrahar Somashekhar	YOTTA1240	4471

25094 7590 10/04/2004

GRAY, CARY, WARE & FREIDENRICH LLP
2000 University Avenue
E. Palo Alto, CA 94303-2248

EXAMINER	
BELLO, AGUSTIN	
ART UNIT	**PAPER NUMBER**
2633	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,343	SOMASHEKHAR, HOSAGRAHAR	
	Examiner	Art Unit	
	Agustin Bello	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-10* is/are allowed.

6)☒ Claim(s) *1-6,11-31 and 33-35* is/are rejected.

7)☒ Claim(s) *32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 11-15, 17-18, 22-29, and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Adam (U.S. Patent No. 6,781,984).

Regarding claim 1, Adam teaches a method for transparently transporting data comprising: converting a first data stream in a first format (reference numeral 202-1 in Figure 2) to a second data stream in a second format (e.g. output of reference numeral 204-1 in Figure 2); transporting the second data stream over a transport medium (reference numerals 206-1, 207, 210 in Figure 2); and converting the second data stream to a third data stream in the first format (e.g. output of reference numeral 218-1 in Figure 2), wherein the third data stream has a substantially identical bit sequence and substantially identical timing as the first data stream (e.g. "preserve data synchronization" in column 2 lines 17-27).

Regarding claims 11 and 23-24, Adam teaches converting a first optical data stream to an electrical data stream (e.g. via reference numeral 204 in Figure 2); transporting the electrical data stream over an electrical transport medium (reference numerals 206-1, 207, 210 in Figure 2); and converting the electrical data stream to a second optical data stream (via reference numeral 218

in Figure 2), wherein the second optical data stream matches the first optical data stream (e.g. "preserve data synchronization" in column 2 lines 17-27).

Regarding claim 12, Adam teaches converting the first data stream to the electrical data stream comprises altering the bit sequence of the first optical data stream (e.g. by inserting idle bytes of column 4 lines 30-40) and formatting the resulting bit sequence for transport over the electrical transport medium (e.g. framing of column 3 lines 5-10), and wherein converting the electrical data stream to the second optical data stream comprises unformatting the electrical data stream and altering the resulting bit sequence of the electrical data stream to match the bit sequence of the first optical data stream (column 3 lines 21-38).

Regarding claims 13 and 25, Adam teaches that the electrical transport medium comprises a switching matrix (reference numeral 210 in Figure 2).

Regarding claim 14, Adam teaches that the electrical network comprises one or more routing devices configured to selectively route the electrical data stream to one of a plurality of potential destination devices (inherent in the switch matrix 210 in Figure 2).

Regarding claim 15, Adam teaches controlling the timing of the second optical data stream to reproduce the timing of the first optical data stream (reference numeral 212, 216 in Figure 2).

Regarding claim 17, Adam teaches that the bit sequence and timing of the second optical data stream matches the bit sequence and timing of the first data stream (column 3 lines 34-38, "preserve data synchronization" in column 2 lines 17-27, and "preserve this data rate" in column 5 lines 2-6).

Regarding claim 18, Adam teaches determining the count of bits per time interval in the first optical data stream (e.g. via reference numeral 630 in Figure 6) and using the count of bits per time interval to reconstruct the timing of the second optical data stream (e.g. via reference numerals 208, 212, 216 in Figure 1).

Regarding claim 22, Adam teaches converting the first optical data stream to the electrical data stream comprises storing data bits corresponding to the first optical data stream in an ingress buffer (reference numeral 207 in Figure 2), counting the number of bits per time interval which are stored in the ingress buffer (reference numeral 630 in Figure 6), storing the number of bits per time interval in the ingress buffer (column 6 lines 21-30) and reading the data bits and corresponding number of bits per time interval out of the ingress buffer (e.g. output of the buffer reference numeral 610 in Figure 6); and wherein converting the electrical data stream to the second optical data stream comprises extracting the number of bits per time interval from the electrical data stream (column 3 lines 34-37), storing the remaining data bits corresponding to the electrical data stream in an egress buffer (reference numeral 214 in Figure 2), reading data bits out of the egress buffer (e.g. output of the buffer 214 in Figure 2) counting the number of bits per time interval which are read out of the egress buffer (column 3 lines 34-37), and adjusting the rate at which data bits are read out of the egress buffer (e.g. via reference numeral 212, 216 in Figure 2) to cause the number of bits per time interval read out of the egress buffer to match the number of bits per time interval extracted from the electrical data stream (e.g. "preserve data synchronization" in column 2 lines 17-27, and "preserve this data rate" in column 5 lines 2-6).

Regarding claim 26, Adam teaches an optical-electrical converter (reference numeral 204 in Figure 2) configured to convert the first optical data stream to the electrical data stream, a buffer (reference numeral 206 in Figure 2) configured to store the electrical data stream, and a counter (reference numeral 630 in Figure 6) configured to count the bits of the data stream which are stored in the buffer.

Regarding claim 27, Adam teaches timing logic (reference numeral 620 in Figure 6) coupled to the counter and configured to determine the number of bits of the data stream which are stored in the buffer during each of a first plurality of regular intervals.

Regarding claim 28, Adam teaches that the timing logic is configured to store a number of counts per interval corresponding to the electrical data stream in the buffer (column 6 lines 21-30).

Regarding claim 29, Adam teaches that the ingress module is configured to convey the data stream and the corresponding number of counts per interval to the egress module (e.g. output via switch matrix 210 in Figure 2).

Regarding claim 35, Adam teaches a first data transport path, wherein the first data transport path comprises a first ingress module (reference numeral 204-1, 206-1, 207-1 in Figure 2) configured to convert optical data stream to a first electrical data stream (reference numeral 204 in Figure 2), a first transmission medium (reference numeral 210 in Figure 2) coupled the ingress module and configured to transport the first electrical data stream, and a first egress module (reference numeral 214-1, 218-1 in Figure 2) configured to receive the electrical data stream form the first transmission medium and to convert the electrical data stream to a second optical data stream (reference numeral 218-1 in Figure 2), wherein the first egress module is

configured reproduce the bit sequence and timing the first optical data stream in the second optical data stream (e.g. "preserve data synchronization" in column 2 lines 17-27, and "preserve this data rate" in column 5 lines 2-6); a second data transport path, wherein the second data transport path comprises second ingress module (reference numeral 204-y, 206y in Figure 2) configured convert a third optical data stream to a second electrical data stream (reference numeral 204-y in Figure 2), a second transmission medium (reference numeral 210 in Figure 2) coupled to the second ingress module and configured to transport the second electrical data stream, and a second egress module (reference numeral 214-y, 218-y in Figure 2) configured to receive the second electrical data stream from the second transmission medium and to convert the second electrical data stream to a fourth optical data stream in a manner which produces a bit sequence in the fourth optical data stream which differs from the third optical data stream (e.g. via the possible switching or routing of bits through reference numeral 210 in Figure 2).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adam in view of Slana (U.S. Patent No. 4,485,468).

Regarding claims 2 and 19, Adam teaches that converting the first data stream to the second data stream comprises periodically determining a data rate for the first data stream (e.g. via counters reference numeral 630-1 in Figure 6) but differs from the claimed invention in that

Adam fails to specifically teach inserting the data rate in the second data stream. However, Slana in the same field of signal switching, teaches it is well known in the art to determine the data rate of a data stream (e.g. via the various counters shown in Figure 1), then insert the data rate into the data stream (e.g. via reference numeral 51 in Figure 1 and shown as reference letter "B" in Figure 3). Furthermore, Adam suggests that information regarding the data rate of the data stream can be written into each of the buffers via known in-band messaging techniques (column 6 lines 21-30). Adam further suggest the ability to insert the data rate into the data stream in that Adam teaches inserting additional overhead bytes into the data stream (column 3 lines 5-10). One skilled in the art would have been motivated to insert the determined data rate into the data stream as suggested by Adam and taught by Slana in order to preserve the data rate throughout the network (column 5 lines 2-6 of Adam) and to accommodate stations having a wide variety of data rates (column 2 lines 35-42). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to determine a data rate for the first data stream, as taught by Adam and Slana, and insert the data rate in the second data stream as suggested by Adam and taught by Slana.

Regarding claim 3, the combination of references and Adam in particular teaches that the data rate is determined by counting (e.g. via reference numeral 630 in Figure 6) a number of bits of the first data stream which are counted in a predetermined interval (e.g. as frames are added to the buffer described in column 7 lines 19-41).

Regarding claim 4, the combination of references and Adam in particular teaches converting the first data stream in a first format to second data stream in a second format further comprises formatting the second data stream in a plurality of frames (column 3 lines 5-10).

Regarding claim 5, the combination of references and Adam in particular teaches converting a first data stream in a first format to second data stream in a second format further comprises formatting the second data stream in a plurality of packets (column 3 lines 5-10 in that frames and packets are synonymous).

Regarding claim 6, the combination of references teaches converting the second data stream to the third data stream comprises extracting the data rate from the second data stream and generating the third data stream at the same data rate (e.g. via reference numeral 216 in Figure 2 of Adam according to Adam's disclosure of "preserving this data rate" of column 5 lines 2-6).

5. Claim 16, 20-21, 30-31, and 33-34 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Adam in view of Caldara (U.S. Patent No. 6,208,667).

Regarding claims 16 and 30, Adam differs from the claimed invention in that Adam fails to specifically teach that controlling the timing of the second optical data stream comprises adjusting the frequency of a phase locked loop configured to control the data rate of the second optical data stream. However, the use of phase lock loops for controlling the timing of data streams is well known in the art. Caldara, in the same field of switching, teaches the use of phase lock loops to control the data rate of optical data streams. One skilled in the art would have been motivated to include phase lock loops to control the data rate of optical data streams in order to regenerate a clock signal thereby allowing the recovery of transmitted data (column 2 lines 35-40). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to include phase lock loops to control the data rate of optical data streams in the system of Adam as taught by Caldara.

Regarding claims 20 and 33, the combination of references teaches generating an internal clock signal (reference numeral 68 in Figure 4 of Caldara), transporting the internal clock signal with the electrical data stream over the electrical transport medium (e.g. via input 69 in Figure 4 of Caldara) and determining data rates associated with the first and second optical data streams based upon the internal clock signal (e.g. via reference numeral 68, 59, and 72 in Figure 4 of Caldara).

Regarding claims 21 and 34, the combination of references teaches providing an external clock signal (reference numeral "REFCLK" in Figure 4 of Caldara) and determining data rates associated with the first and second optical data streams based upon the external clock signal (e.g. via reference numeral 68, 59, and 72 in Figure 4 of Caldara).

Regarding claim 31, the combination of references and Adam in particular teaches timing logic (reference numeral 216 in Figure 2) coupled to the counter and configured to determine the number of bits of the data stream which are read out of the buffer during each of a second plurality of regular intervals.

Allowable Subject Matter

6. Claims 7-10 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach or fully suggest a system for transparently transporting data comprising: an ingress module configured to convert a first data stream to an second data stream, wherein the ingress module comprises an ingress buffer configured to store the first data stream, an ingress counter configured to count the bits of the first data stream which are stored in the ingress buffer an ingress timer, and write logic coupled to the ingress counter and the ingress timer and configured to determine the data rate of the first data stream, wherein the write logic is further configured to periodically write the data rate of the first data stream into the ingress buffer; an egress module configured to receive the second data stream and to convert the second data stream to a third data stream, wherein the egress module is configured to reproduce the bit sequence and timing of the first data stream in the third data stream, wherein the egress module comprises an egress buffer configured to store the second data stream, a phase locked loop (PLL) configured to control the rate at which data is read out of the egress buffer to produce the third data stream, an egress counter configured to count the bits of the third data stream, timing logic coupled to the egress counter and the egress timer and configured to determine the data rate the third data stream and to control the PLL to match rate of third stream to the data stream; a

transport medium coupled between the ingress module and the egress module and configured to convey the second egress module.

8. Claim 32 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Adam and Urbansky teach relevant art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Agustin Bello whose telephone number is (571) 272-3026. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Agustin Bello
Examiner
Art Unit 2633

AB

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600